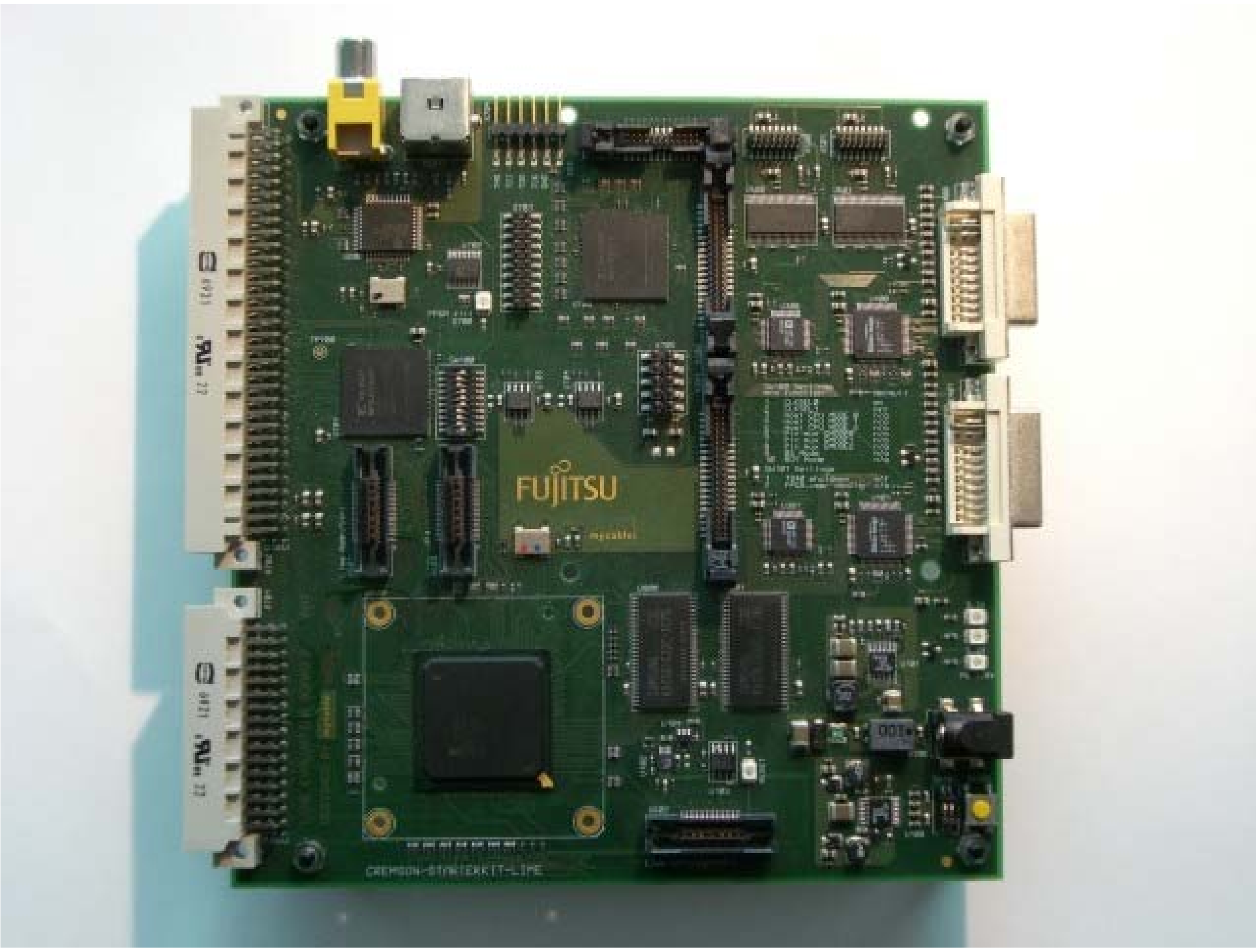
CREMSON-STARTERKIT-LIME Rev. 1.03

Feb 2007

1.03

Lime Evaluation Board



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Document Revision History

Revision Number	Date	Description of changes
1.00	25/10/05	Preliminary
1.01	06/01/06	First Version for Board Revision PA6
1.02	09/01/07	Added note for proprietary board designs and errata, general information update and minor corrections
1.03	19/02/07	Corrected GMODE table

Evaluation Board Revision History

Revision Number	Date	Description of changes
PA5	30/11/05	First Board Version PA5
PA7	13/01/06	Revised version - adds SW102 for Lime reset - changes thermal pins to VCC18

CONTENTS

1 Overview

The CREMSON-STARTERKIT-LIME is a low-cost multifunctional evaluation board for Fujitsu's MB86276 'Lime' Graphic Controller. The board is a part of a modular system and is connected to the 'CREMSON-STARTERKIT-CPU-Modul' board as a simple target board for both software development and testing, allowing design engineers to begin with software development immediately before their proprietary (final) target system is available.

2 MB86276 'Lime' Features

- CMOS 0.18µm technology
- Internal and memory frequency : 133MHz
- Base-clock for display clocks : 400.9MHz
- Display resolutions typically from 320x240
- 6 layers of overlay display (windows)
- Alpha Plane and constant alpha value
- Digital Video input (various formats
- Video Scaler (up/down scaling)
- Brightness, Contrast, Saturation control
- RGB digital output (8bit x 3)
- Built-in alpha blending, anti-aliasing
- Rendering Engine for various kinds
- Texture Mapping Unit for 2D polygon
- Bit-Blt Unit for transfers up to 4096x4096
- Alpha Bit-Blt and ROP2 functions
- External 32-bit SDRAM interface for
- Parallel host interface (FR, SH3, SH4)
- New additional serial control interface
- Internal and external DMA support
- I2C interface and GPIO inputs/outputs
- Supply voltage 3.3V (I/O), 1.8V (Internal)
- BGA-256 Package (1.27mm pitch)
- Typical power consumption < 1.0W
- Temperature range -40..+85 °C

3 System Components

This diagram provides a functional overview of the system (note that it does not give a true representation of the physical board – e.g. the FPGA device is actually two FPGA's).

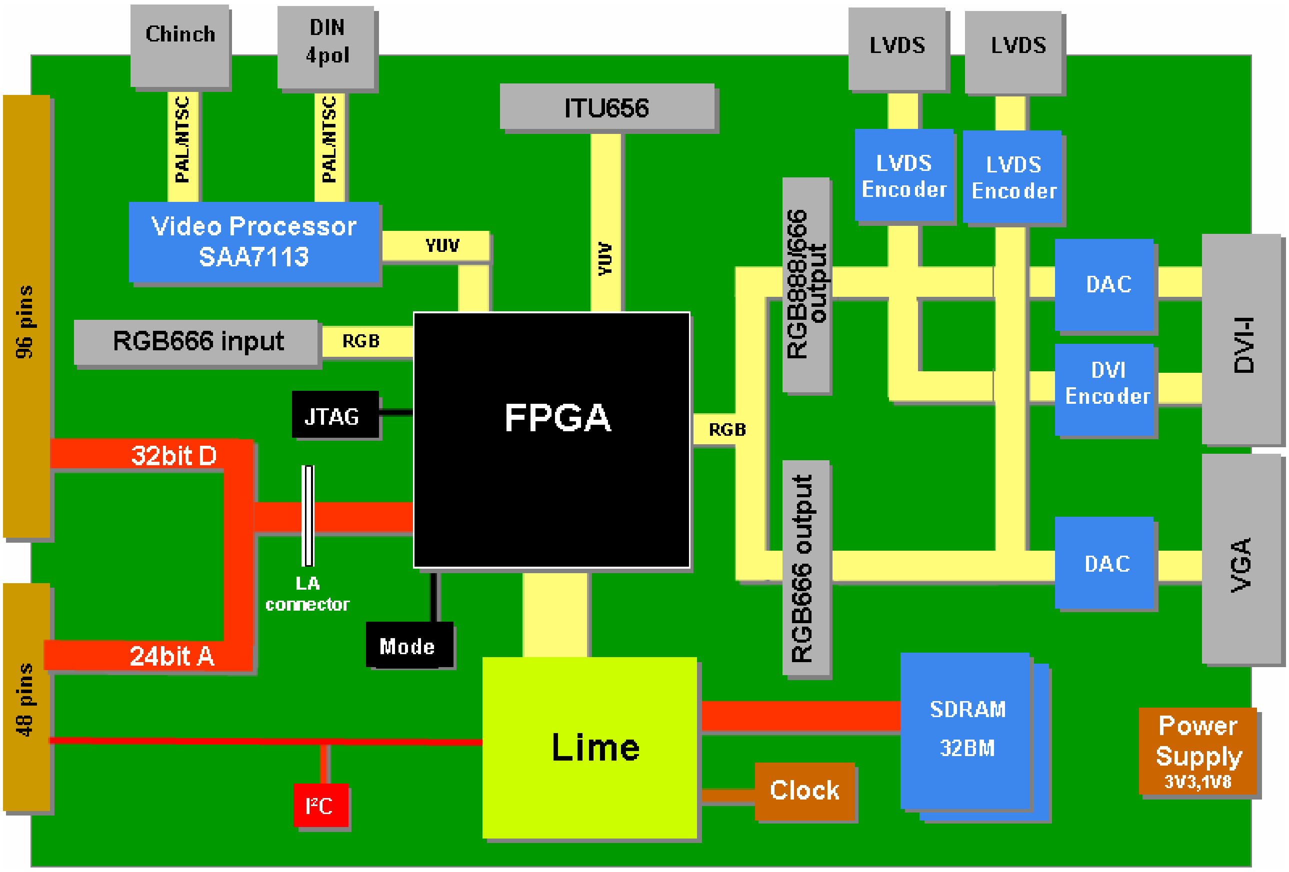


Figure 1 Functional Block Diagram

The main components and interfaces of the CREMSON-STARTERKIT-LIME evaluation board:

- Lime Graphic Controller
- 64Mbytes SDRAM
- Video outputs
  - 2 x DVI
  - 2 x RGB digital
  - 2 x LVDS
- Video inputs
  - Digital RGB666
  - Digital YUV422 (ITU656)
  - CVBS
  - S-Video
- Others
  - Xilinx FPGA's
  - Test LED's
  - Configuration settings

4 Layout and Interface Location

The location of the various interfaces of the board (the outline of which is shown below) is best determined using the current schematics (in this document) and the physical board's silkscreen markings. Locate the connector's ID (e.g. X703) in the schematics and then check the silkscreen markings on the physical board.

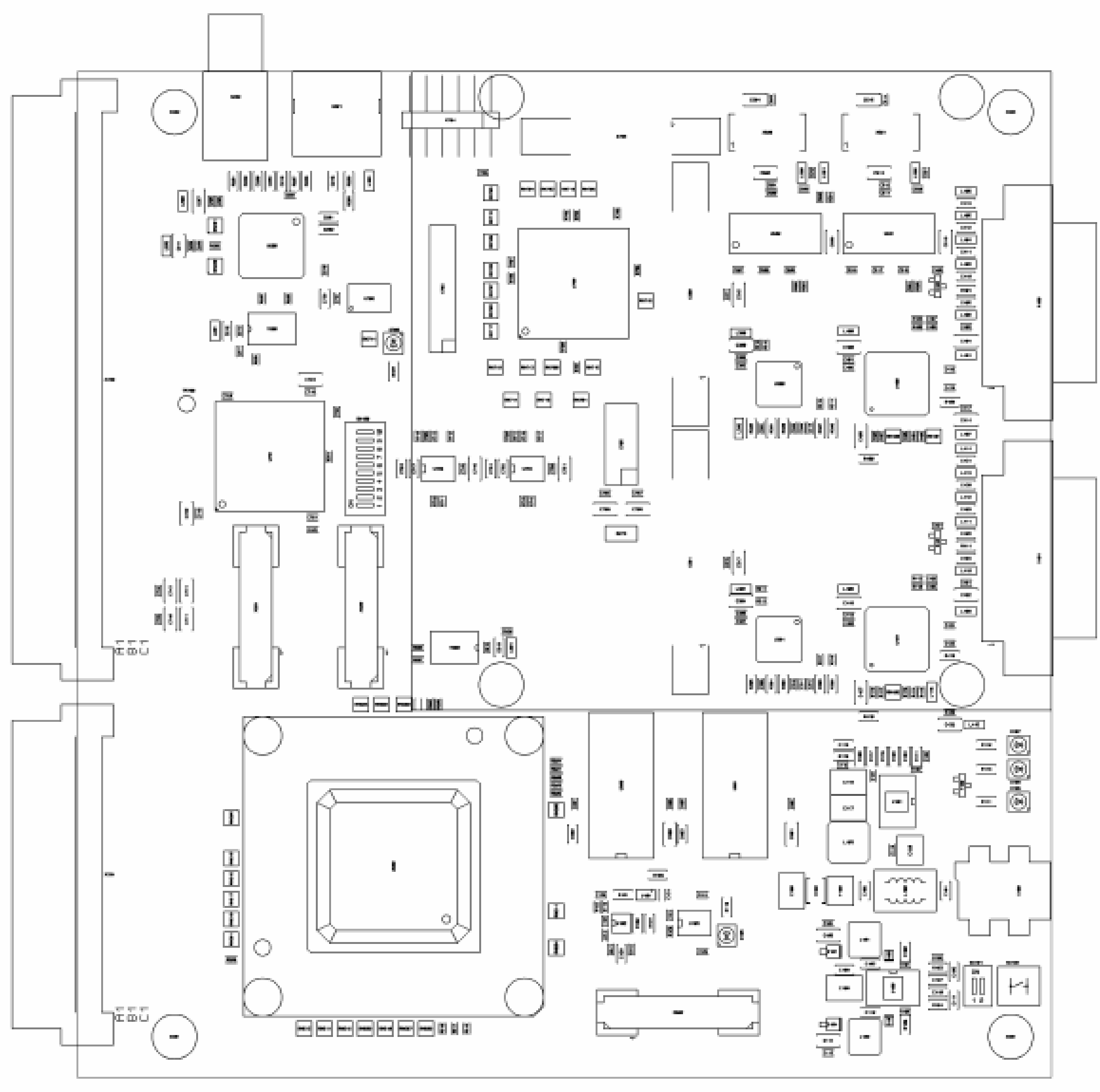


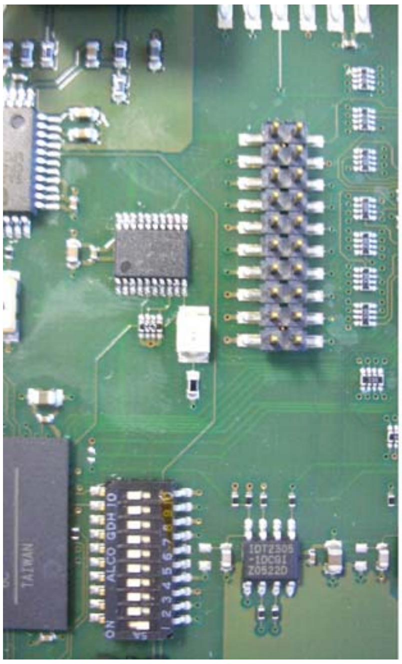
Figure 1 Interfaces of the Lime evaluation board

5 Power Status LED's

LED's are connected to the power nets of the board and therefore an illuminated LED shows the availability of its corresponding power net. The power LED's are located at the lower right corner of the board, the Reset LED under the external SDRAM and the FPGA power LED near the video input.

LED	Function	Description
D105	Reset	(Red) Reset level active
D106	1.8V supply	(Green) 1.8V power supply
D107	3.3V supply	(Green) 3.3V power supply
D108	5.0V supply	(Green) 5.0V power supply
D700	3.3V supply	(Red) 3.3V power supply

Table 1 Power Status LED's



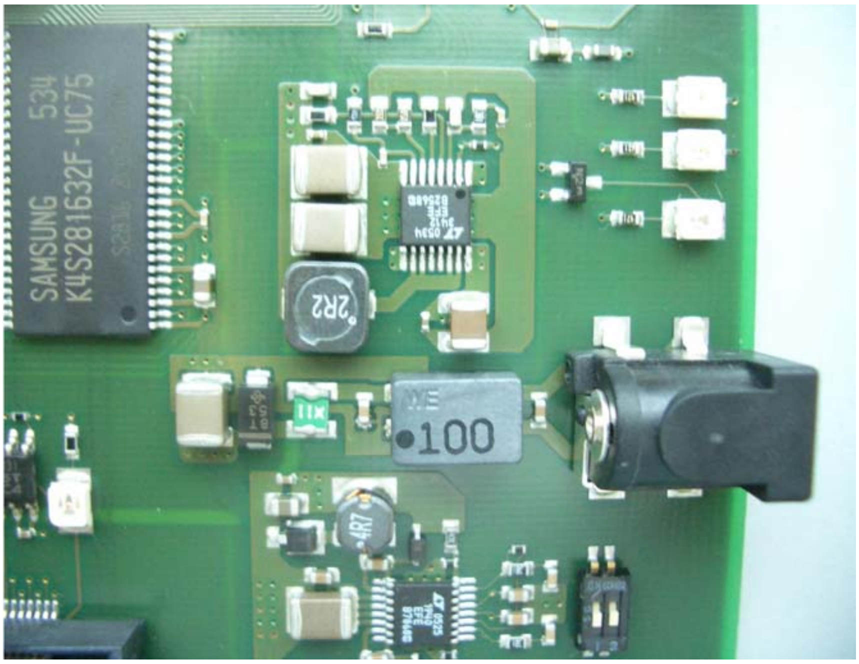


Figure 2 Power Status LED's

6 Configuration DIP Switches

The table shows DIP switches SW100 and SW101 of the Lime evaluation board. These should be configured according to the intended host CPU interface mode and output display connection. Before connecting the evaluation board for the first time, make sure that all switches are correctly set. Possible settings and defaults are shown below.

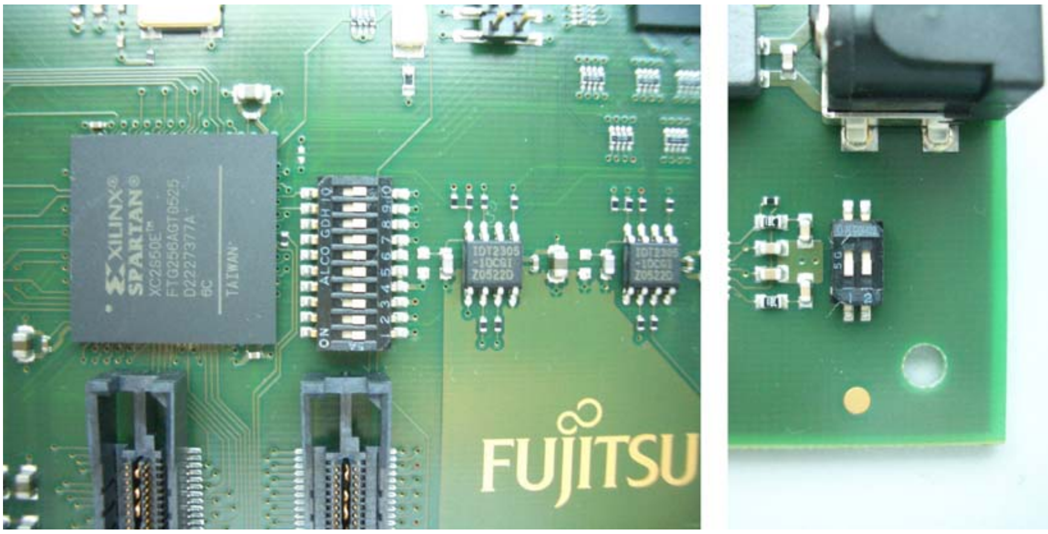


Figure 3 Configuration DIP Switches

DIP switch	Function	Set	Description
SW100-1	CLKSEL0	ON	Other oscillator settings
		OFF	14.32 MHz source (Default)
SW100-2	CLKSEL1	ON	14.32 MHz source (Default)
		OFF	Other oscillator settings
SW100-3	CPU MODE 0	ON	Host CPU mode select[1]
		OFF	
SW100-4	CPU MODE 1	ON	
		OFF	
SW100-5	CPU MODE 2	ON	
		OFF	
SW100-6	MUX GMODE 0	ON	General purpose mode pins[2]
		OFF	
SW100-7	MUX GMODE 1	ON	
		OFF	
SW100-8	MUX GMODE 2	ON	
		OFF	
SW100-9	BS Mode	ON	Connects to CPU with BS signal
		OFF	Connects to CPU without BS signal
SW100-10	RDY Mode	ON	Sets the XRDY signal to the 'not ready' level
		OFF	Sets the XRDY signal to the 'ready' level
SW101-1	Switching Regulator shutdown	ON	Switch On
		OFF	Switch Off
SW101-2	FPGA configuration	ON	Reserved
		OFF	

[1],[2] Check the CPU mode and the General Purpose Mode tables in the hardware manual (see also below).

For Hardware Manual cross-reference purposes: (see following sections)
ON = Low
OFF = High

6.1 CLKSEL0/CLKSEL1

The following table (copied from the MB86276 'Lime' Hardware Manual available at the time this document was written) lists the CLKSEL settings that can be selected.

CLKSEL1	CLKSEL0	Input frequency	Assured operation range (*1)
L	L	13.5 MHz	13.365 to 13.5 MHz
L	H	14.32 MHz	14.177 to 14.32 MHz
H	L	17.73 Hz	17.553 to 17.73 MHz
H	H	33.33 Hz	32.997 to 33.33 MHz

Table 2 Clock Select

*1 Assured operation input frequency range: Standard value –1%

6.2 CPU Mode

The following table (copied from the MB86276 'Lime' Hardware Manual available at the time this document was written) lists the CPU modes that can be selected.

CPU MODE 2	CPU MODE 1	CPU MODE 0	CPU
L	L	L	SH3 **(Fujitsu FR series MCU's)**
L	L	H	SH4
L	H	L	V832
L	H	H	SPARClite
H	L	L	General purpose 16bit CPU with SRAM interface
H	L	H	General purpose 16bit CPU with address and data multiplex interface
H	H	L	General-purpose 32bit CPU with address and data multiplex interface
H	H	H	I2C Slave

Table 3 CPU Modes

6.3 General Purpose Mode Pins

The following table (copied from the MB86276 'Lime' Hardware Manual available at the time this document was written, talking the Errata Sheet nto consideration) lists the General Purpose modes that can be selected and the pin multiplex functionality that results (note also the dependency on the corresponding CPU mode listed in the previous section).

MUX GMODE 2	MUX GMODE 1	MUX GMODE 0	PIN Multiplex				
			Host Interface	Primary RGB output	Secondary RGB output	Video Capture	GPIO
L	L	L	32bit CPU I2C Slave	RGB888	--	Native RGB666	--
L	L	H	32bit CPU I2C Slave	RGB888	--	RBT656/601	GPIO[4:0]
L	H	L	16bit CPU I2C Slave	RGB666	RGB888	RBT656/601	GPIO[2:0]
L	H	H	16bit CPU I2C Slave	RGB666	RGB666	Native RGB666	--
H	L	L	Reserved	Reserved	Reserved	Reserved	Reserved
H	L	H	Reserved	Reserved	Reserved	Reserved	Reserved
H	H	L	Reserved	Reserved	Reserved	Reserved	Reserved
H	H	H	Reserved	Reserved	Reserved	Reserved	Reserved

Table 4 Multiplex Modes

7 Interfaces and connectors

7.1 Connectors between CPU board and graphic board

This section describes the connector allocation between the CPU board and the graphic board. The connection of the two sub-boards is realized by two connectors: a 96-pole DIN plug and a 48-pole DIN plug.

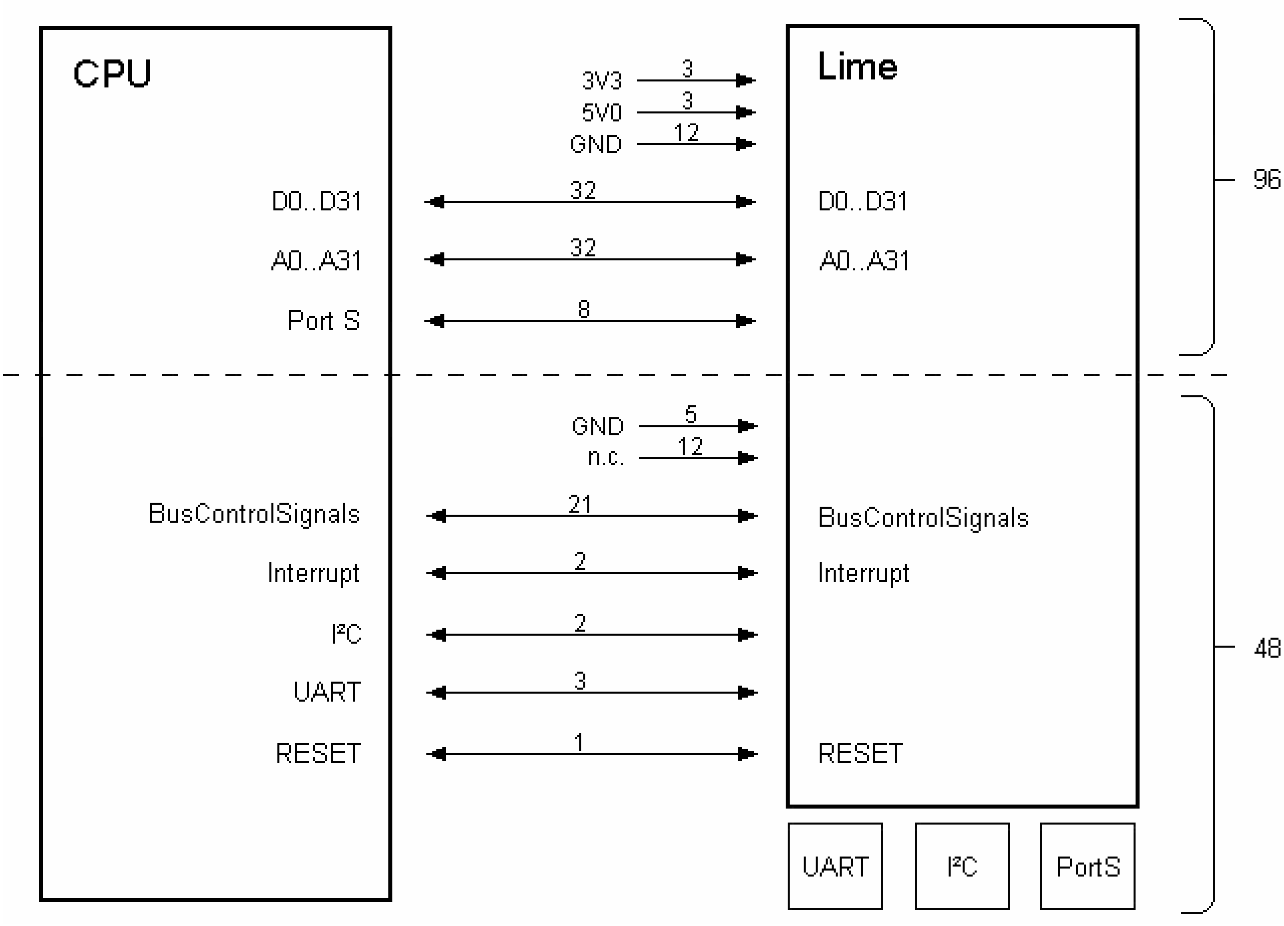


Figure 3 Connection Block Diagram

Pin	Name
A1	n.c.
A2	3.3V
A3	5.0V
A4	GND
A5	D0
A6	D3
A7	D6
A8	D9
A9	D12
A10	D15
A11	D18
A12	D21
A13	D24
A14	D27
A15	D30
A16	GND
A17	A0
A18	A3
A19	A6
A20	A9
A21	A12
A22	A15
A23	A18
A24	A21
A25	A24
A26	n.c.
A27	n.c.
A28	S0
A29	S3
A30	S6
A31	n.c.
A32	GND

Pin	Name
B1	n.c.
B2	3.3V
B3	5.0V
B4	GND
B5	D1
B6	D4
B7	D7
B8	D10
B9	D13
B10	D16
B11	D19
B12	D22
B13	D25
B14	D28
B15	D31
B16	GND
B17	A1
B18	A4
B19	A7
B20	A10
B21	A13
B22	A16
B23	A19
B24	A22
B25	A25
B26	n.c.
B27	n.c.
B28	S1
B29	S4
B30	S7
B31	n.c.
B32	GND

Pin	Name
C1	n.c.
C2	3.3V
C3	5.0V
C4	GND
C5	D2
C6	D5
C7	D8
C8	D11
C9	D14
C10	D17
C11	D20
C12	D23
C13	D26
C14	D29
C15	GND
C16	GND
C17	A2
C18	A5
C19	A8
C20	A11
C21	A14
C22	A17
C23	A20
C24	A23
C25	n.c.
C26	n.c.
C27	GND
C28	S2
C29	S5
C30	GND
C31	n.c.
C32	GND

Table 5 96-Pole Connector Pin*[1] Reference

Pin	Name	Pin	Name	Pin	Name
A1	CS0	B1	GND	C1	CS1
A2	CS2	B2	1.8V	C2	CS3*[2]
A3	CS4	B3	GND	C3	CS5
A4	CS6	B4	1.8V	C4	RDY
A5	BGRNT	B5	GND	C5	BRQ
A6	RDX	B6	n.c.	C6	WR0
A7	WR1	B7	n.c.	C7	WR2
A8	WR3	B8	n.c.	C8	AS
A9	ALE	B9	n.c.	C9	CLK
A10	DREQ0	B10	n.c.	C10	DACK0
A11	DEOP0	B11	n.c.	C11	n.c.
A12	IRQ_A	B12	n.c.	C12	SDA
A13	IRQ_B	B13	n.c.	C13	SCL
A14	SIN	B14	n.c.	C14	SOT
A15	GND	B15	n.c.	C15	SLK
A16	RESET	B16	n.c.	C16	GND

Table 6 48-Pole Connector Pin*[1] Reference

*[1] Note:
The pin number refers to the female connector of the CPU main board.

*[2] Note:
CS3: This is currently used by the FR 467 and 369 CPU's in connection with the Lime device.

7.2 Interface for the digital RGB output

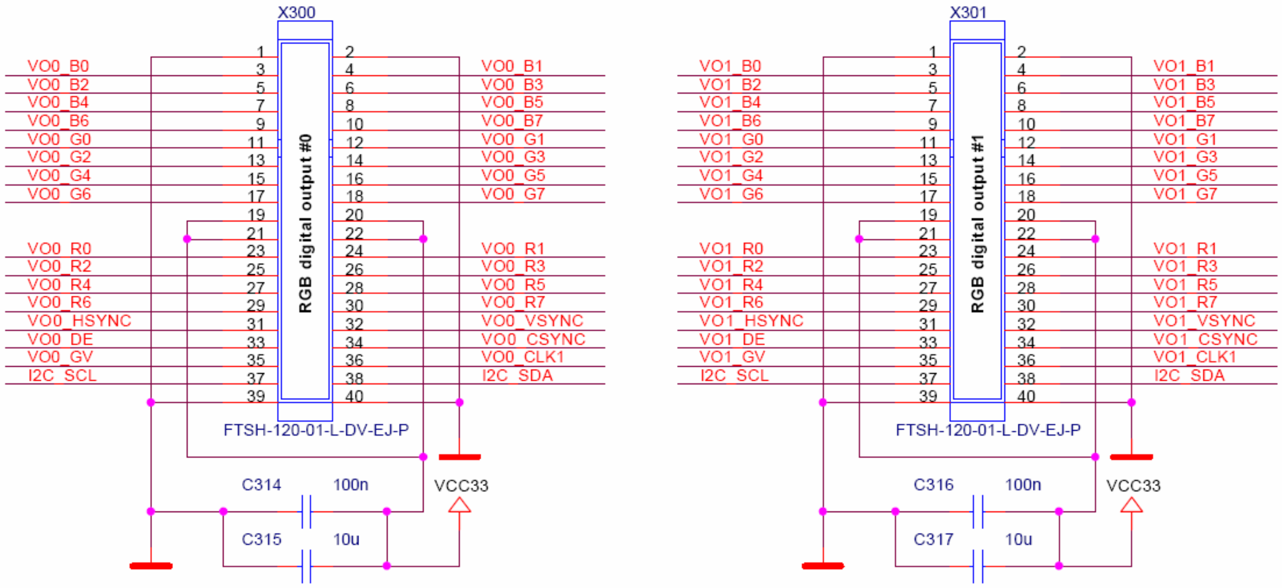


Figure 6 Digital RGB out

7.3 Interface for LVDS out



Figure 7 LVDS out

7.4 Interface for the digital RGB input

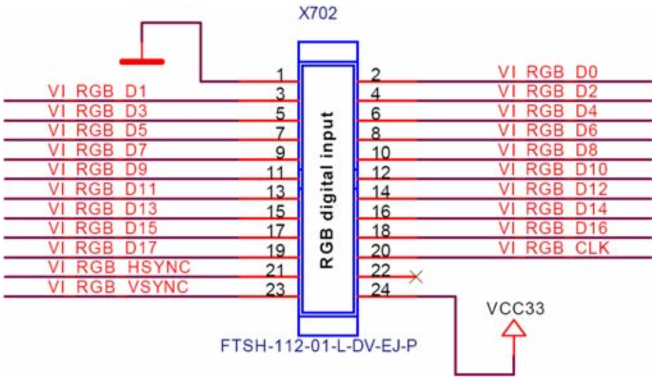
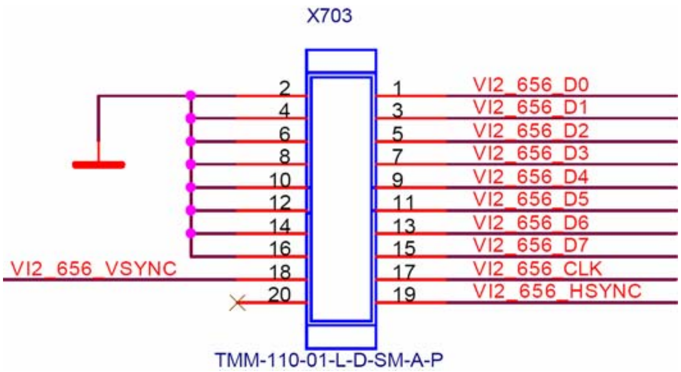


Figure 8 Digital RGB in

7.5 Interface for the digital YUV422 input



RGB digital input

Figure 9 Digital YUV422 (ITU656) input

8 Schematic Lime Evaluation Board (PA7)

Please refer to the pages following the Fujitsu Headquarters address information.

9 Important Notes for Proprietary Board Designs

- **Address line remapping via FPGA**
  Customers who wish to use Lime in legacy 32-bit modes (SH3, SH4, V832, and FR) and may want to simplify the situation by directly mapping Lime's host interface to the host interface connector should be aware that the FPGA on the Starterkit maps the CPU's address bus lines to those of the Lime device with an offset according to the CPU type.
  For 16 bit CPU's the offset is 1 (i.e. line 1 of the address bus is mapped to line 0 of Lime).
  For 32 bit CPU's the offset is 2 (i.e. line 2 of the address bus is mapped to line 0 of Lime).

- **Direct Access to Graphics Memory**
  If you are trying to access Lime on the Starterkit board from your own CPU board, direct access to graphics memory can be very critical in verifying CPU-Lime communication. Also, if you want to use Local Memory Transfer of display lists to store bitmaps in graphics memory etc. direct access to the Graphics Memory is necessary. This requires modified FPGA firmware which can be obtained by contacting the GCC Application Group (gdc_info@fme.fujitsu.com).

- **Using a non-Fujitsu CPU board / Component Initialization via I2C**
  I2C master communication using the Lime device is not possible for the slave devices SAA7113 and DVI Panel Link Translator. These slave devices should therefore be initialized through I2C using the host interface (i.e. the MCU must control the peripheral directly).

10 Errata

- **Incorrect silkscreen board markings/comments in schematics**
  The silkscreen description and schematic comments for the settings of SW100 are incorrect for the PA7 version of the board. The table lists the default settings as follows:

CLKSEL0	Default ON
CLKSEL1	Default OFF

The correct settings are: (14.32 MHz)

CLKSEL0	Default OFF
CLKSEL1	Default ON

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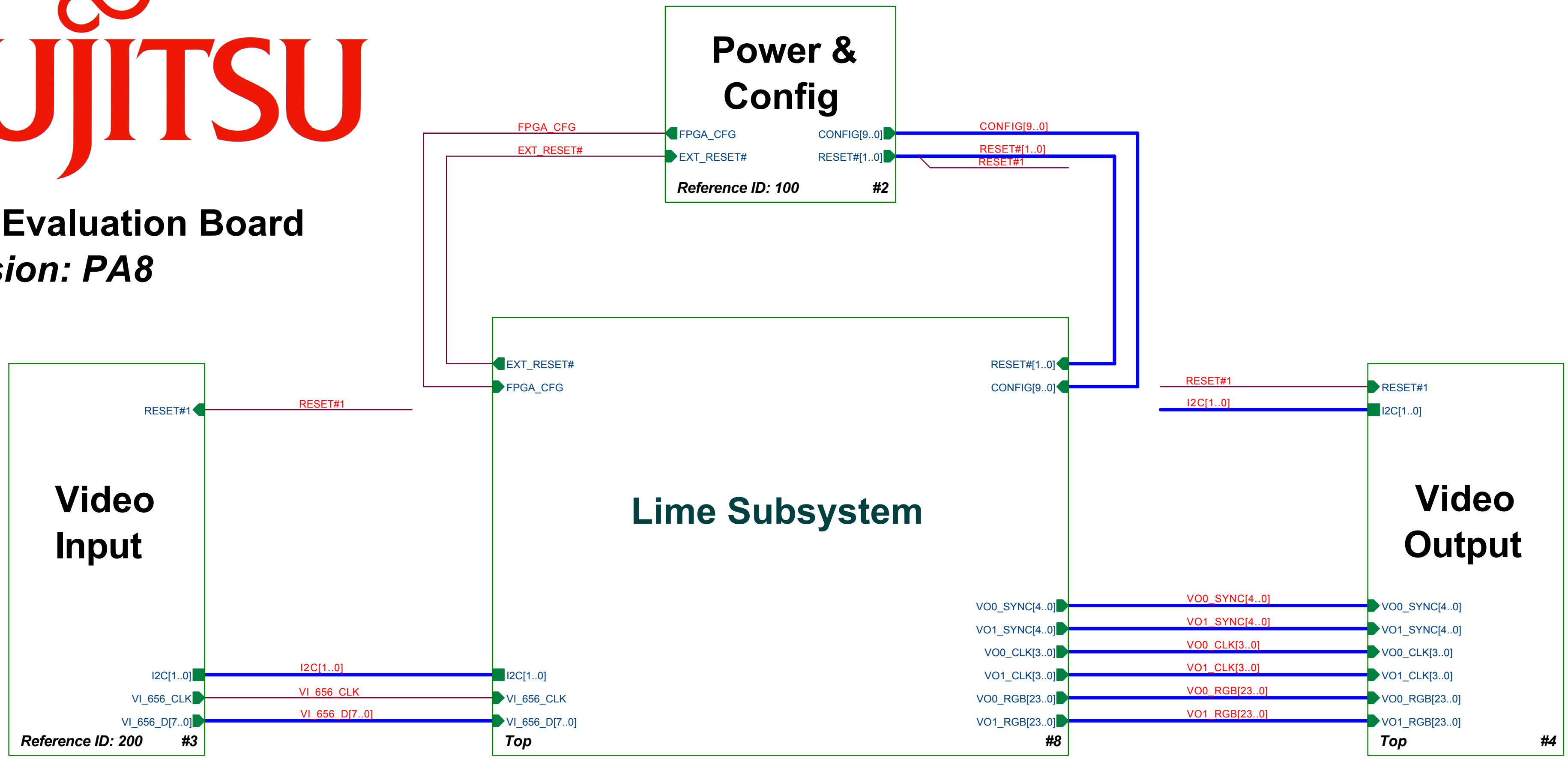
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Lime Evaluation Board

Revision: PA8



Lime Evaluation Board

Hierarchy	Part References
+---#1 Lime Eval Top	
+---#2 Power	1xx
+---#3 Video Input	2xx
+---#4 Video Output	
+---#5 RGB Output	3xx
+---#6 DVI Output	4xx
+---#7 LVDS Output	5xx
+---#8 Lime Subsystem	
+---#9 Lime	6xx
+---#10 FPGA	7xx
+---#11 DRAM	8xx

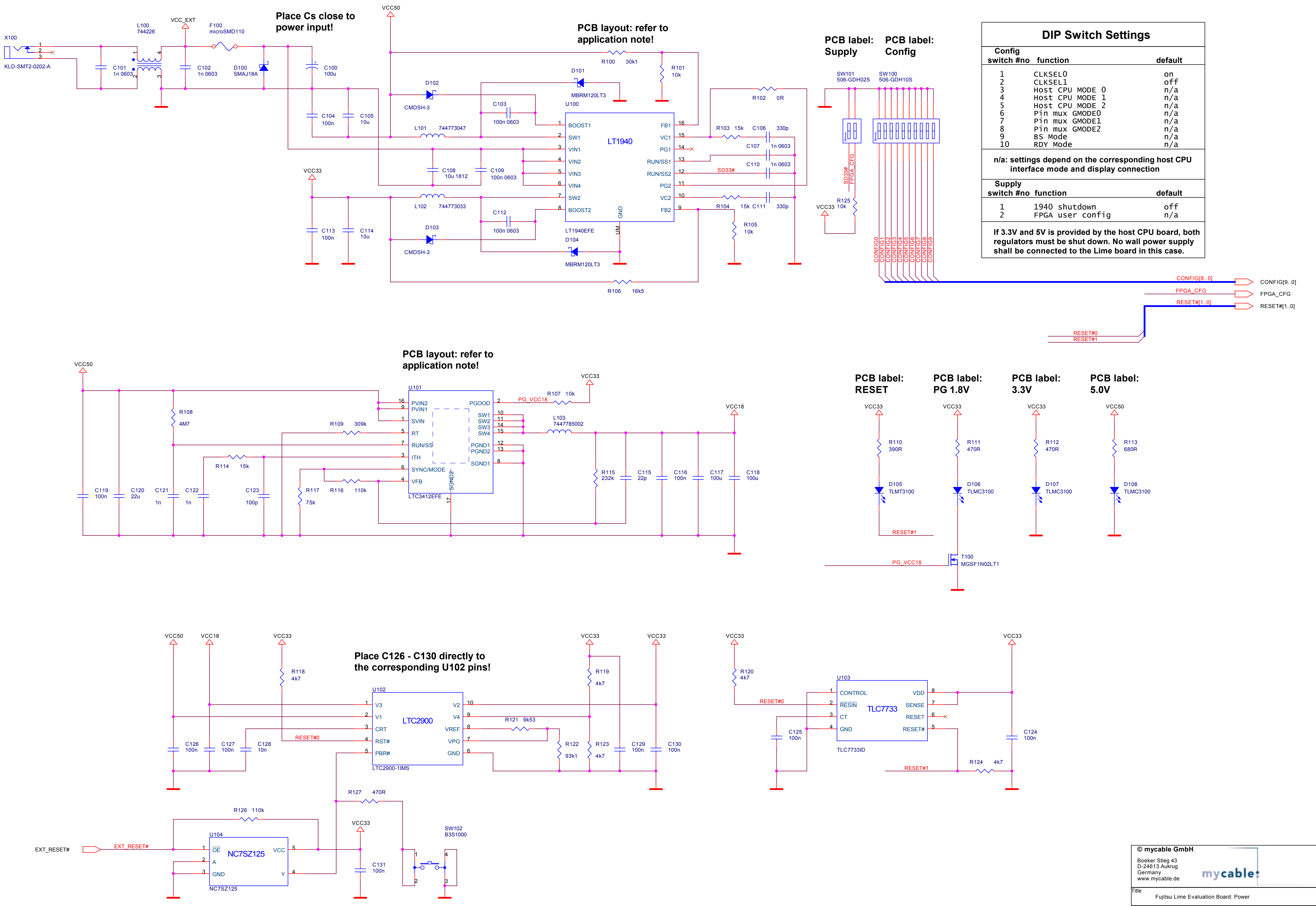
I2C Address Map

Device	Function	Write	Read
Ux00 SAA7113	composite video input	0x48	0x49
Ux00 XC2S200E*	video input selector and host CPU bus mux	0x60	0x61
Ux00 SIL164	DVI transmitter #0	0x70	0x71
Ux01 SIL164	DVI transmitter #1	0x72	0x73

* I2C address of video input selector depends on FPGA implementation

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DIP Switch Settings

Config switch #no	function	default
1	CLKSEL0	on
2	CLKSEL1	off
3	Host CPU MODE 0	n/a
4	Host CPU MODE 1	n/a
5	Host CPU MODE 2	n/a
6	Pin mux GMODE0	n/a
7	Pin mux GMODE1	n/a
8	Pin mux GMODE2	n/a
9	BS Mode	n/a
10	RDY Mode	n/a

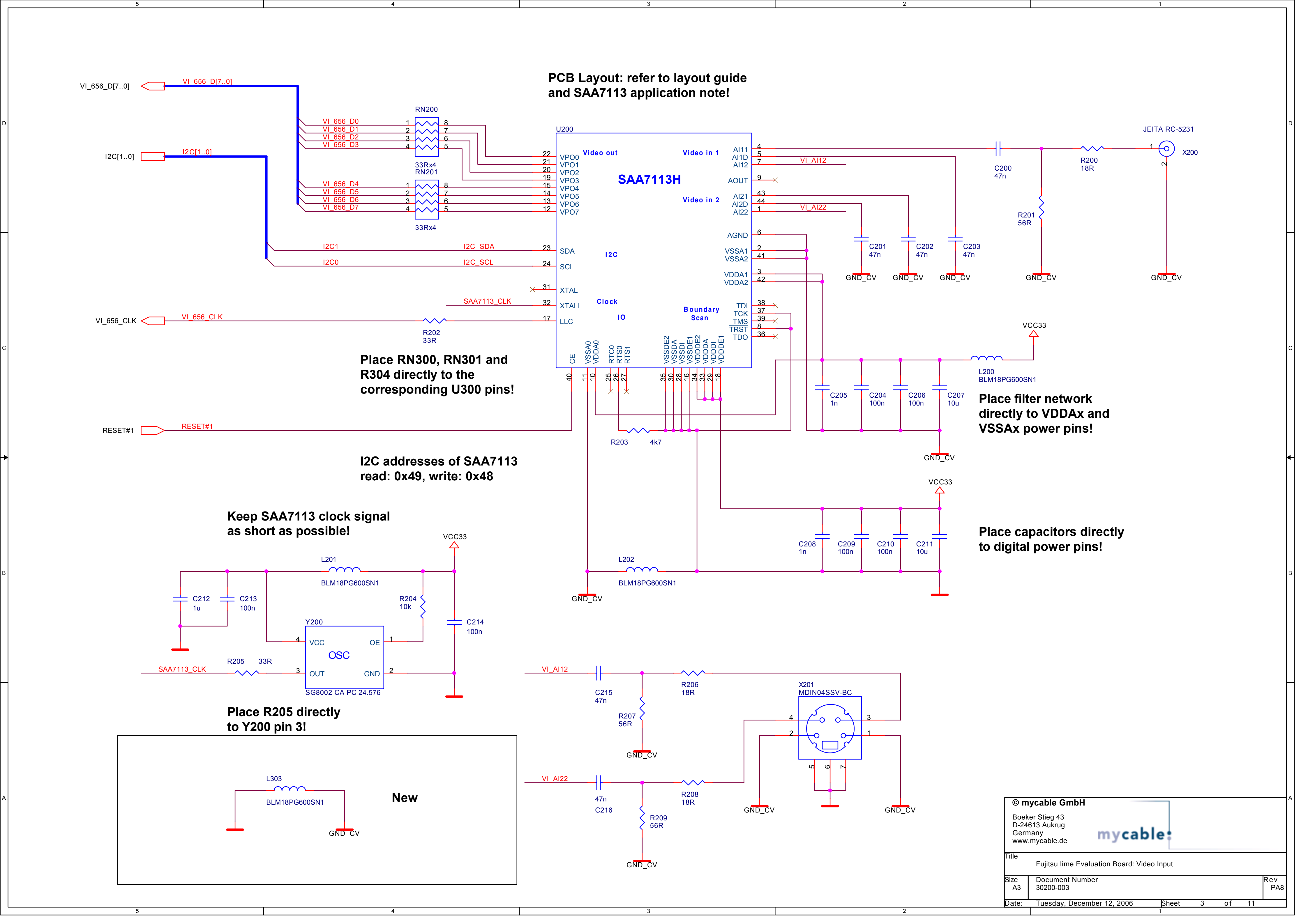
n/a: settings depend on the corresponding host CPU interface mode and display connection

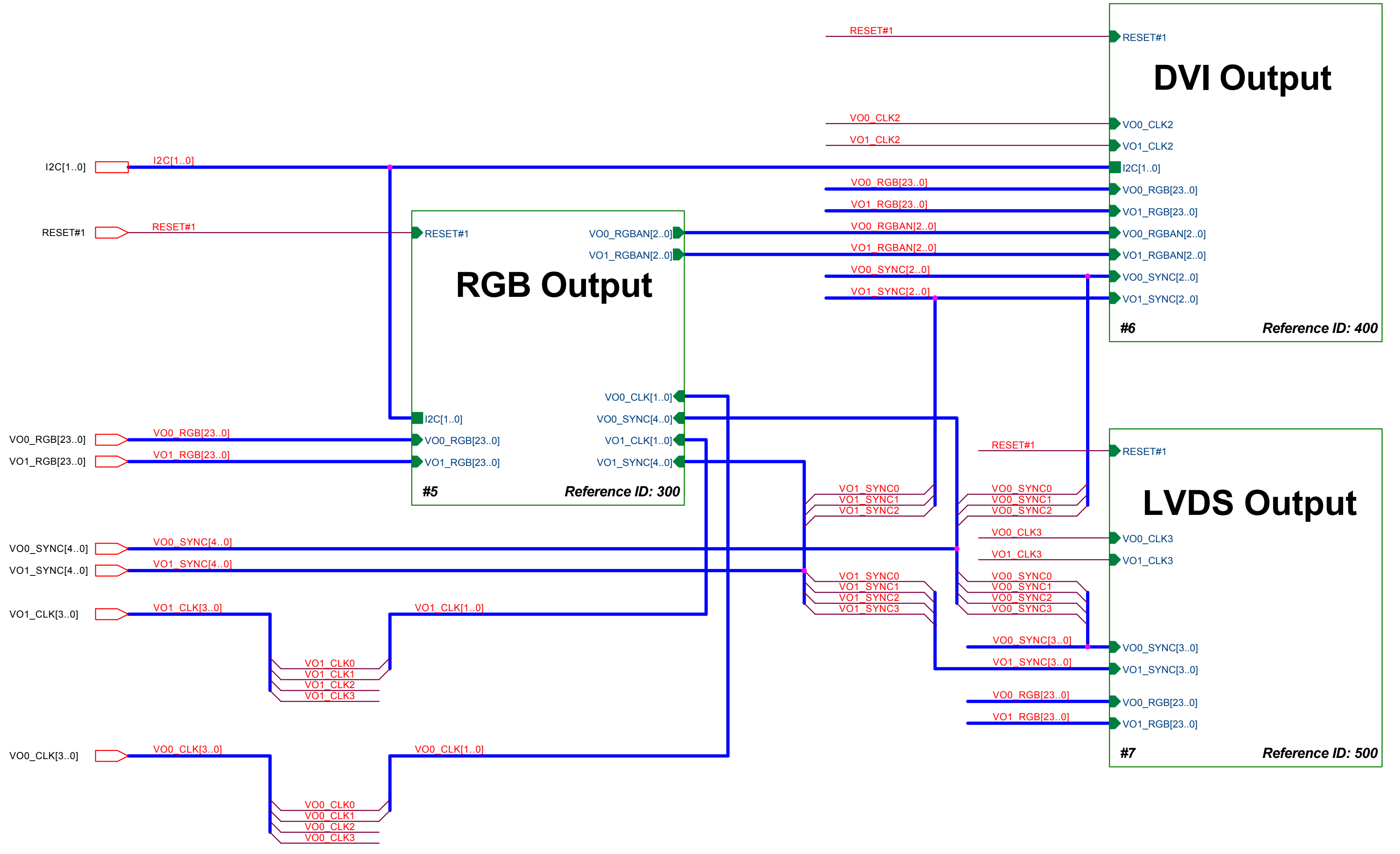
Supply switch #no	function	default
1	1940 shutdown	off
2	FPGA user config	n/a

If 3.3V and 5V is provided by the host CPU board, both regulators must be shut down. No wall power supply shall be connected to the Lime board in this case.

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Title	Fujitsu Lime Evaluation Board: Power
Size	A2
Document Number	30200-002
Rev	PA8
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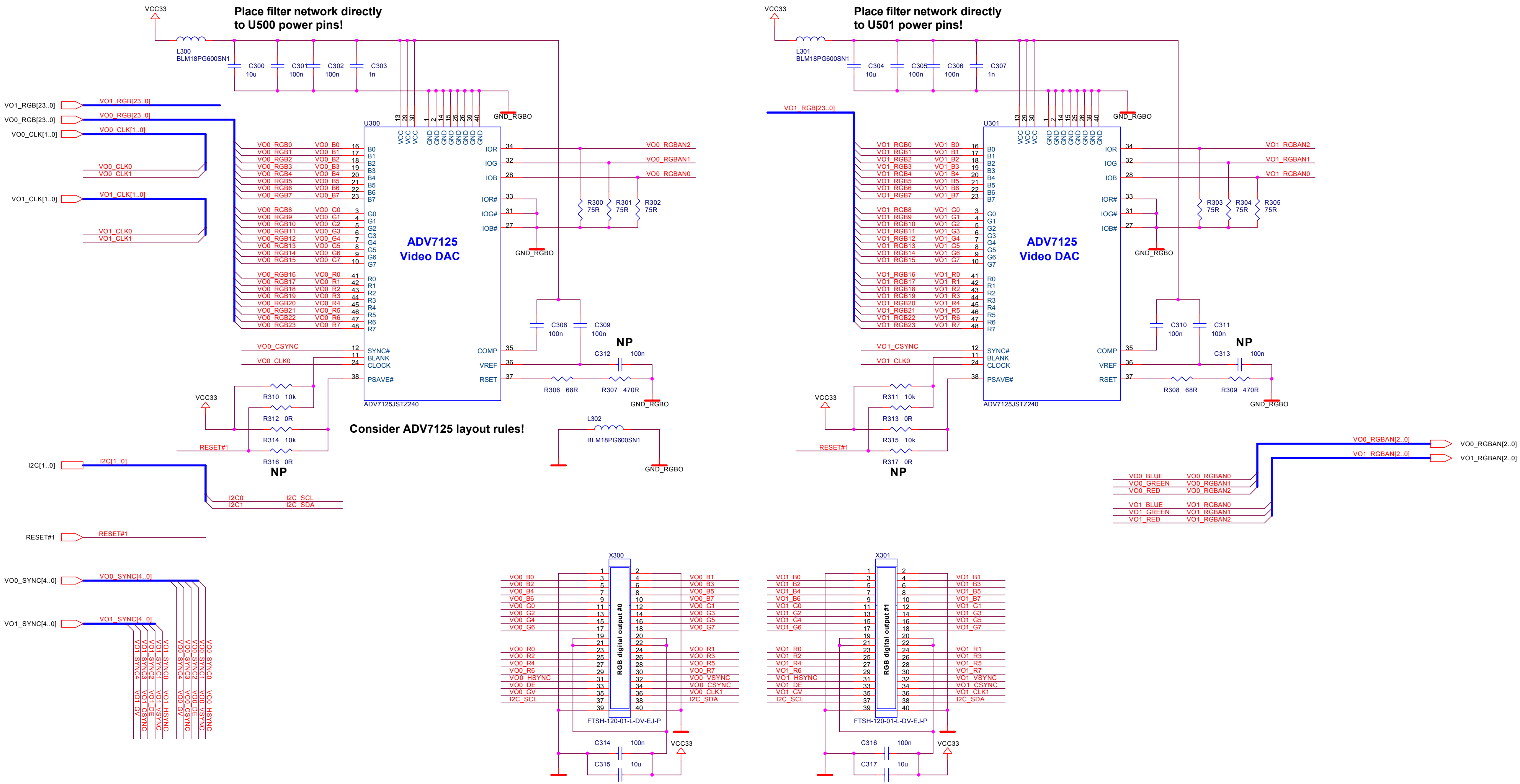

PCB Layout: refer to layout guide
and SAA7113 application note!
VI_656_D[7..0]
I2C[1..0]
VI_656_CLK
RESET#1
RN200
33Rx4
RN201
33Rx4
U200
SAA7113H
Video out
Video in 1
Video in 2
I2C
Clock
IO
Boundary Scan
VPO0
VPO1
VPO2
VPO3
VPO4
VPO5
VPO6
VPO7
SDA
SCL
XTAL
XTALI
LLC
AI11
AI1D
AI12
AOUT
AI21
AI2D
AI22
AGND
VSSA1
VSSA2
VDDA1
VDDA2
TDI
TCK
TMS
TRST
TDO
CE
VSSA0
VDDA0
RTC0
RTS0
RTS1
VSSDE2
VSSDA
VSSDI
VSSDE1
VDDDE2
VDDDA
VDDDI
VDDDE1
I2C_SDA
I2C_SCL
SAA7113_CLK
R202
33R
R203
4k7
JEITA RC-5231
X200
C200
47n
R200
18R
R201
56R
C201
47n
C202
47n
C203
47n
GND_CV
VCC33
L200
BLM18PG600SN1
C205
1n
C204
100n
C206
100n
C207
10u
Place RN300, RN301 and
R304 directly to the
corresponding U300 pins!
Place filter network
directly to VDDAx and
VSSAx power pins!
I2C addresses of SAA7113
read: 0x49, write: 0x48
Keep SAA7113 clock signal
as short as possible!
L201
BLM18PG600SN1
C212
1u
C213
100n
R204
10k
C214
100n
Y200
OSC
VCC
OE
OUT
GND
SG8002 CA PC 24.576
R205
33R
Place R205 directly
to Y200 pin 3!
L202
BLM18PG600SN1
C208
1n
C209
100n
C210
100n
C211
10u
Place capacitors directly
to digital power pins!
VI_AI12
VI_AI22
C215
47n
R206
18R
R207
56R
C216
47n
R208
18R
R209
56R
X201
MDIN04SSV-BC
L303
BLM18PG600SN1
New
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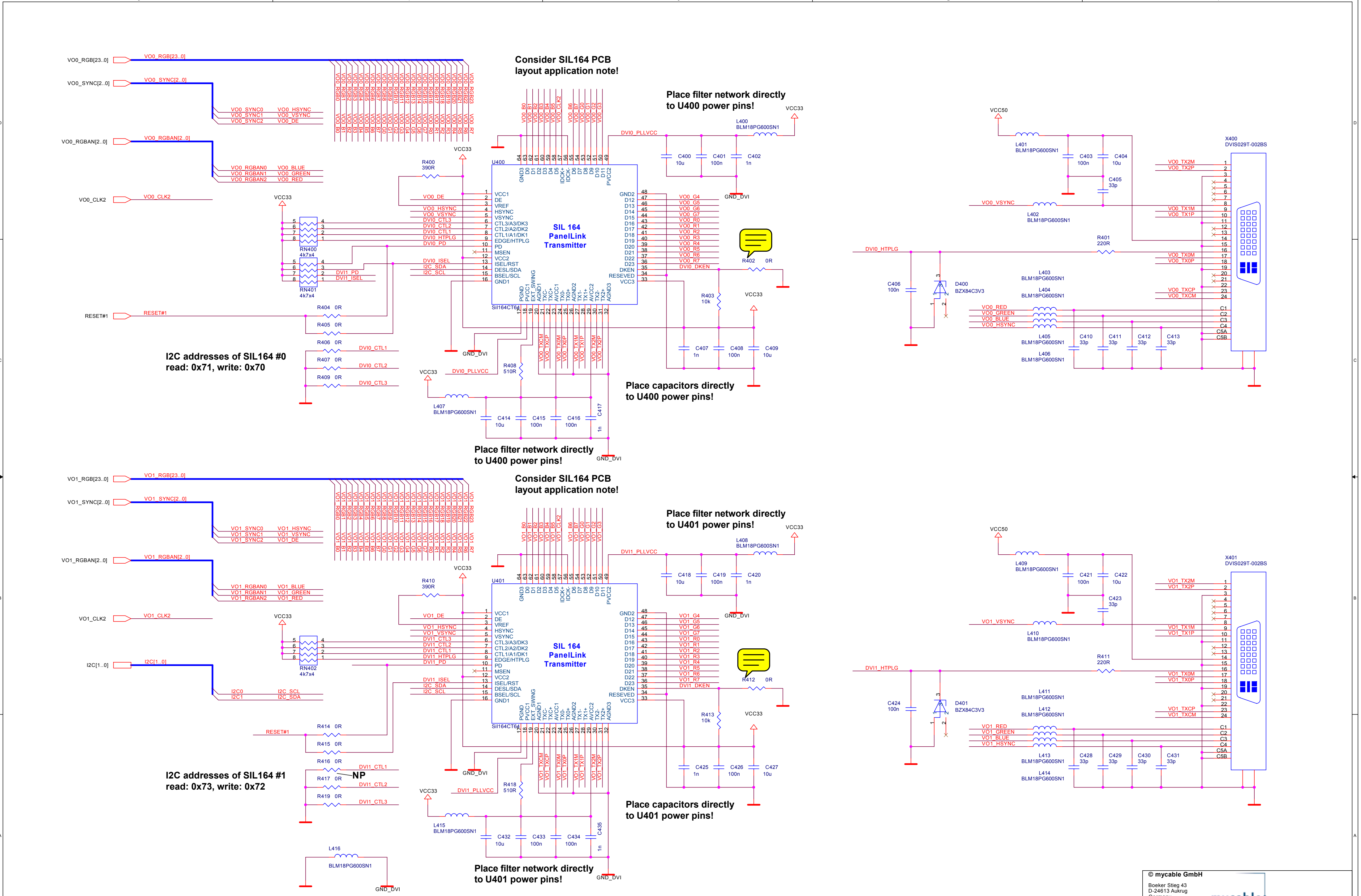
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Size: A3	Document Number: 30200-004		Rev: PA8
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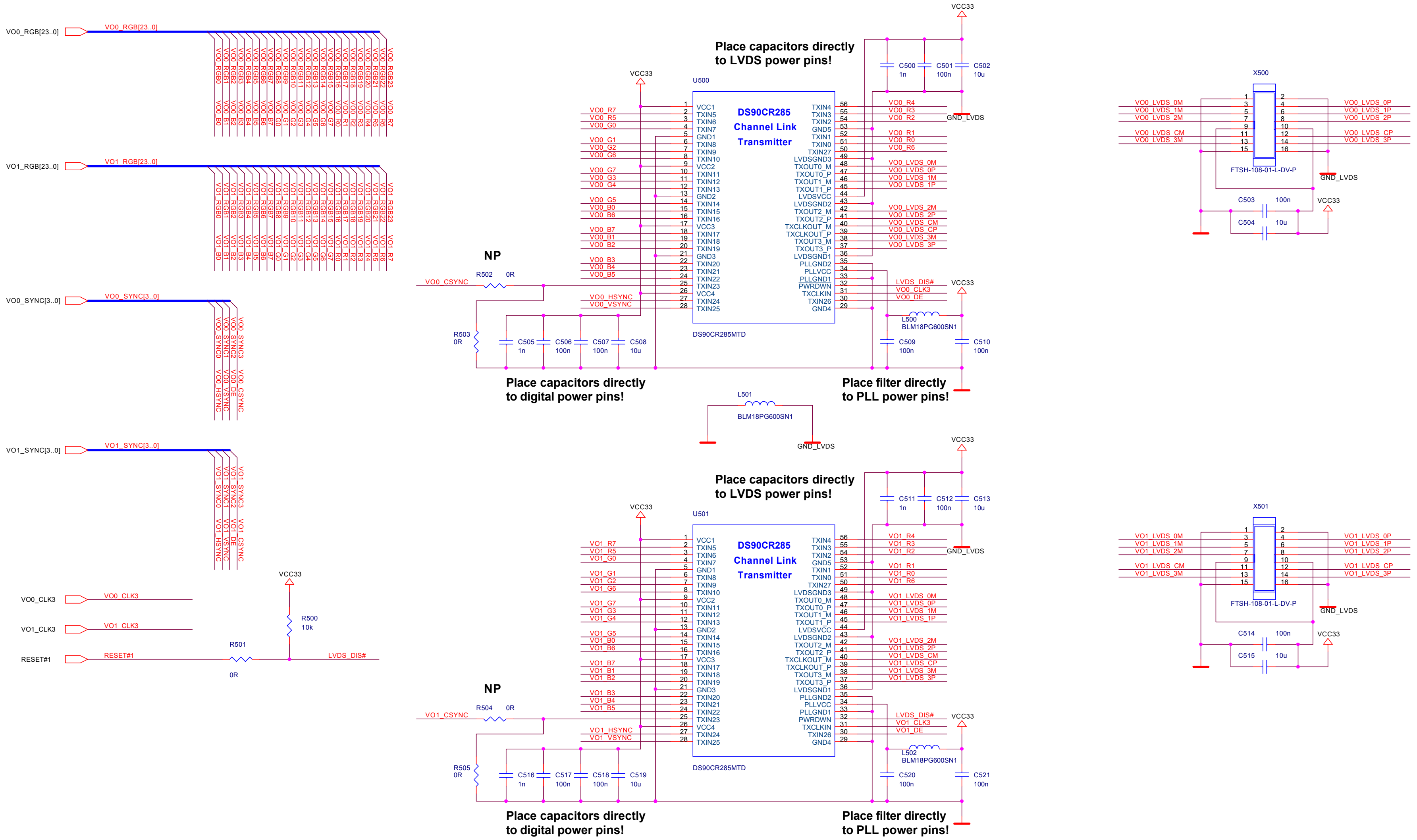
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Title: Fujitsu Lime Evaluation Board: Video Output: DVI Output

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A2	30200-006	PA8

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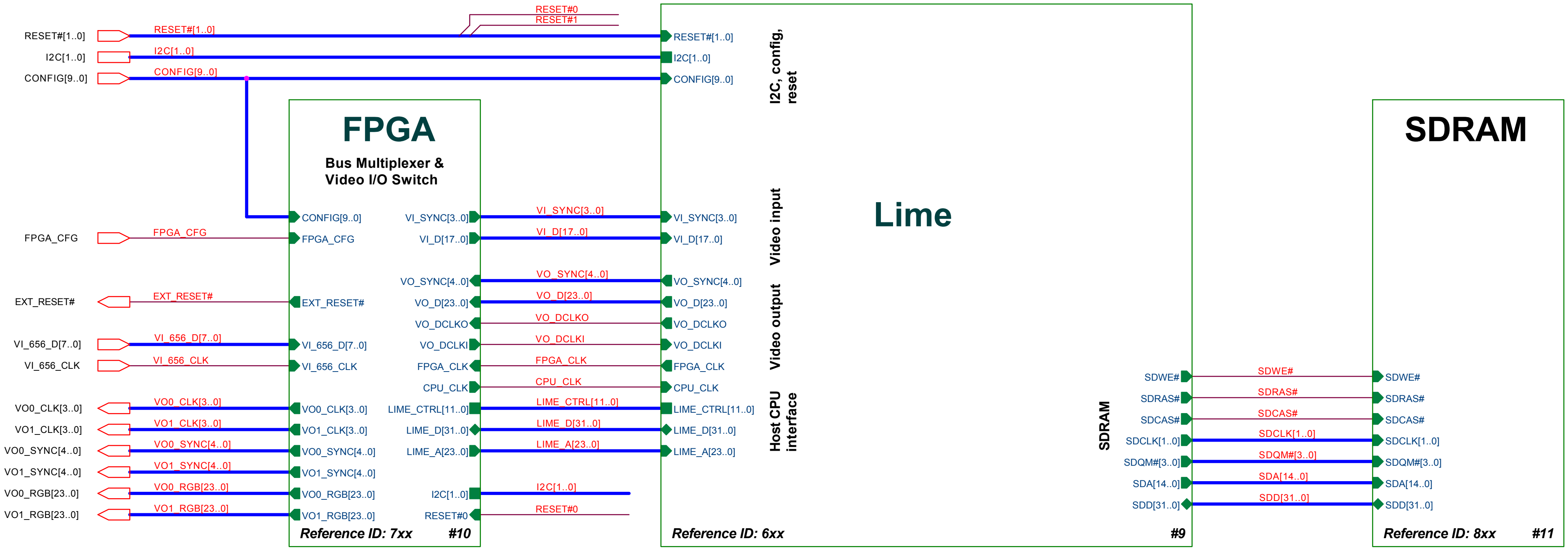
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Title: Fujitsu Lime Evaluation Board: Video Output: LVDS Output

Size	Document Number	Rev
A2	30200-007	PA8

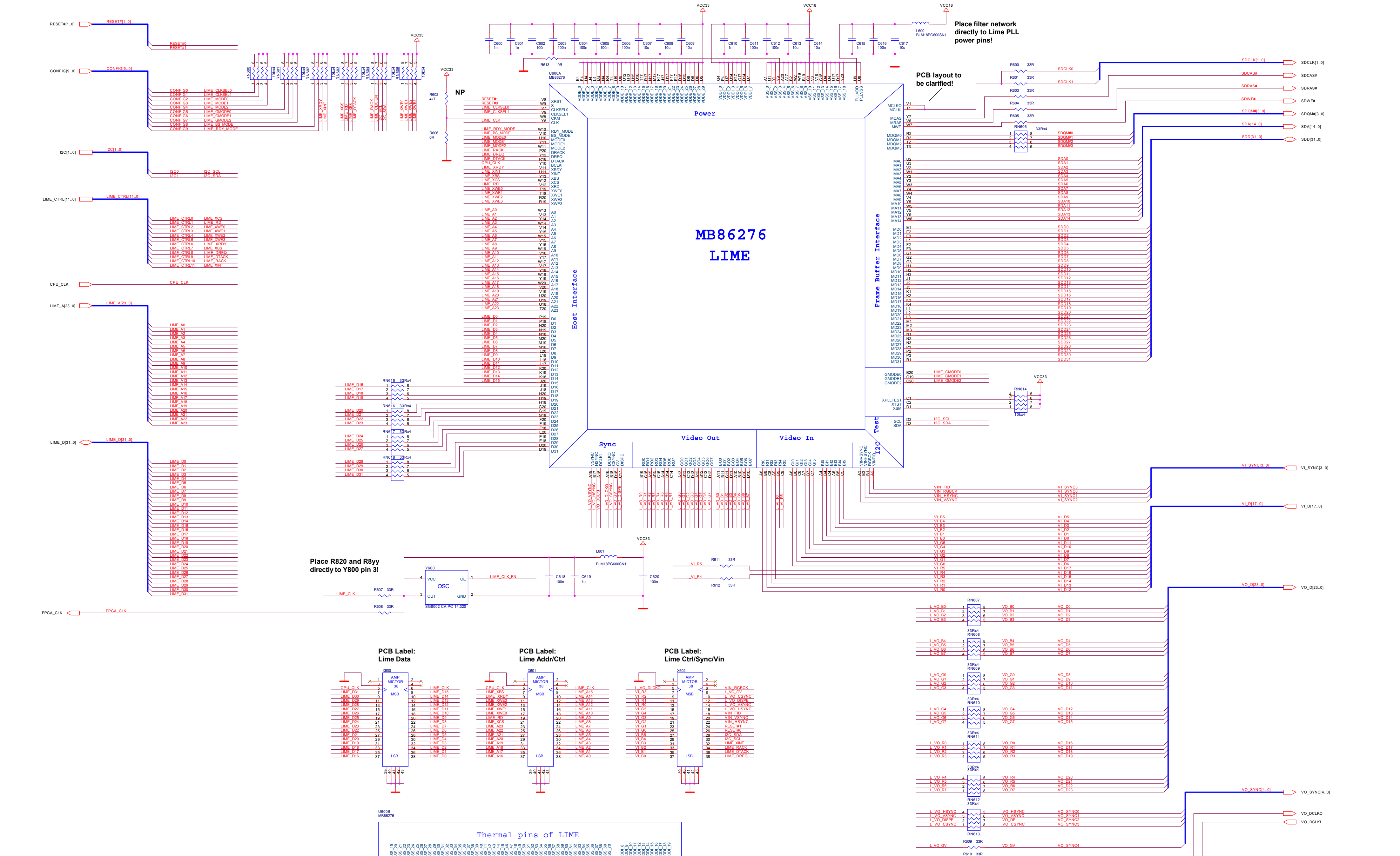
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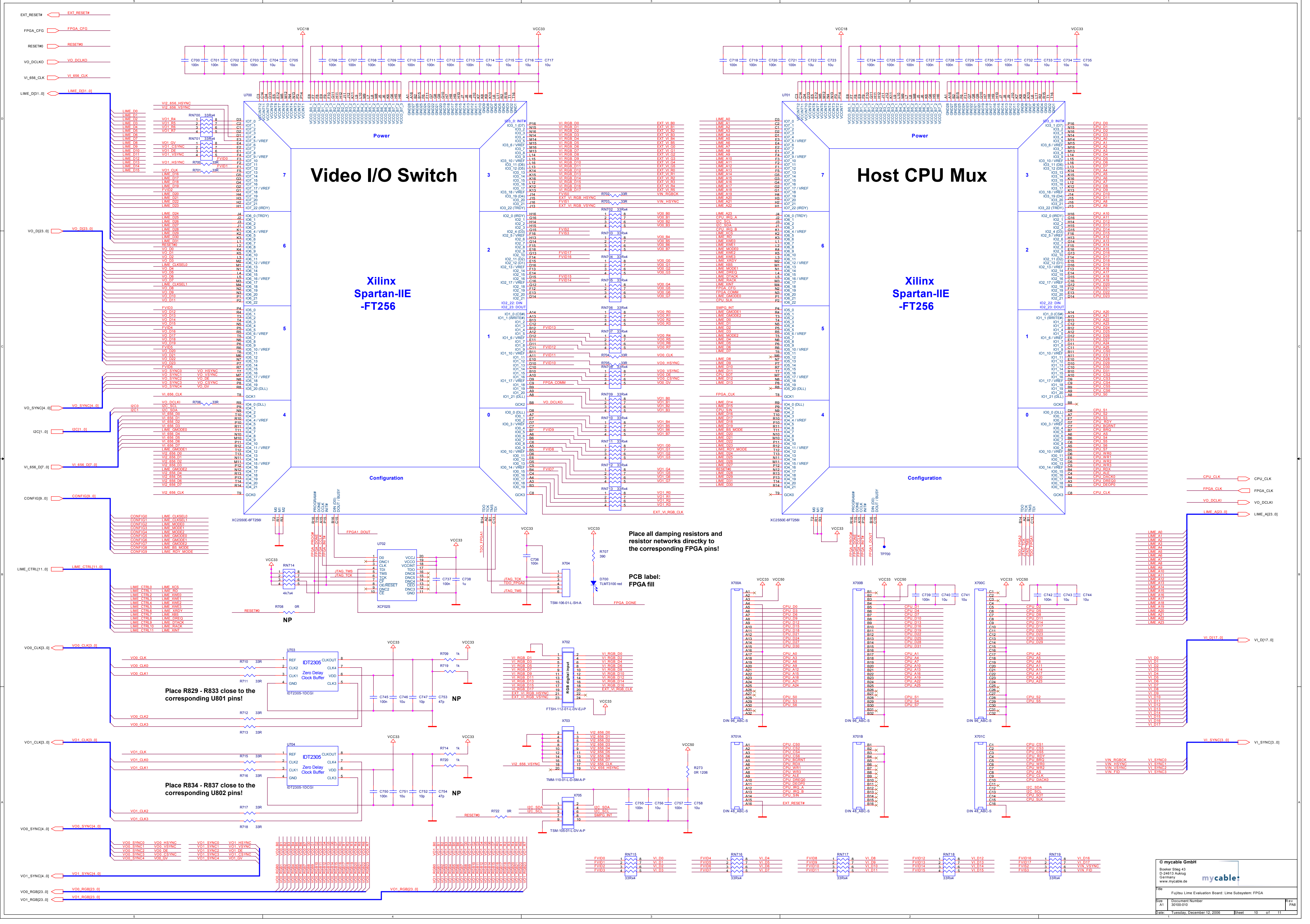
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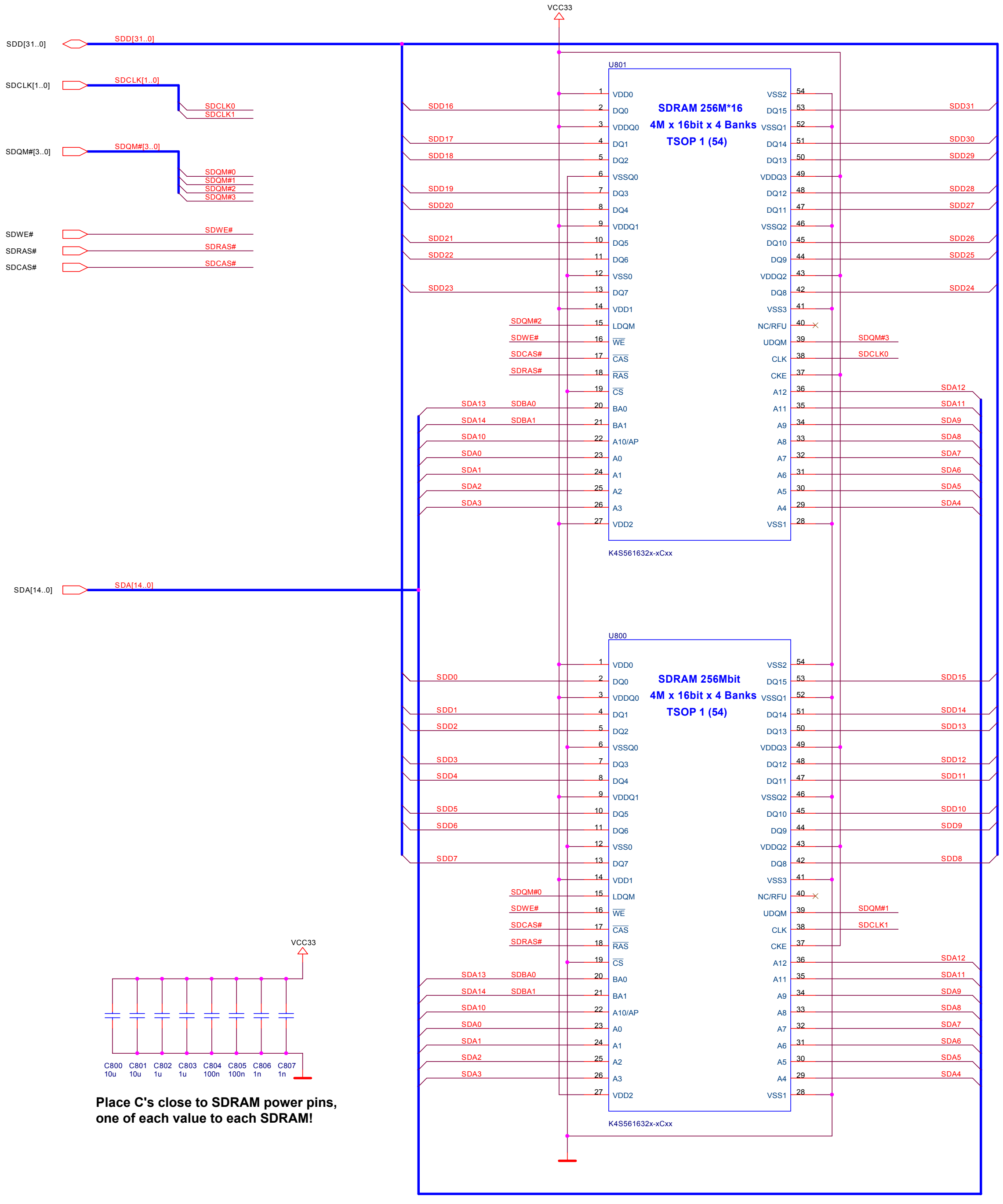
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Title	Fujitsu Lime Evaluation Board: Lime Subsystem: Lime
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Video I/O Switch
Xilinx
Spartan-IIE
-FT256
Host CPU Mux
Xilinx
Spartan-IIE
-FT256
Power
Configuration
Power
Configuration
Place all damping resistors and
resistor networks directky to
the corresponding FPGA pins!
PCB label:
FPGA fill
Place R829 - R833 close to the
corresponding U801 pins!
Place R834 - R837 close to the
corresponding U802 pins!
NP
IDT2305
Zero Delay
Clock Buffer
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